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(71) Applicant:
LUCENT TECHNOLOGIES INC.
Murray Hill, New Jersey 07974-0636 (US)

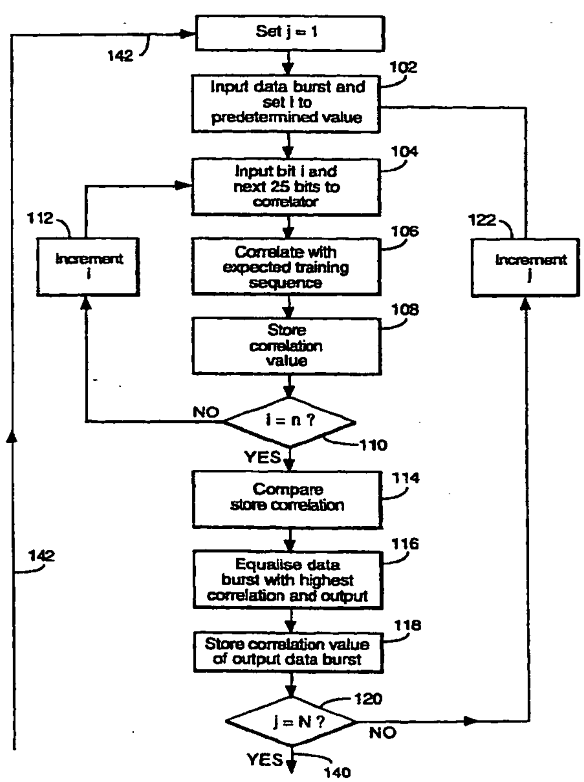
(72) Inventor: Zhou, Hai
Swindon, Wiltshire SN5 6JZ (GB)

(74) Representative:
Williams, David John et al
Lucent Technologies UK Limited,
5 Mornington Road
Woodford Green, Essex IG8 0TU (GB)

(54) Timing estimation for GMS bursts based on previously determined average values

(57) There is disclosed a method and apparatus for estimating the timing position of data bursts received in a data stream, where each data burst includes a number of bits comprising a training sequence in a fixed location. The receiver includes circuitry for estimating the timing position of the data bursts received in the data stream. For each of the first N received data bursts, the receiver estimates a plurality of timing locations of the training sequence, correlates the training sequence for each estimated timing location, and determines the timing location associated with the highest correlation value. The receiver then determines the average timing location of the highest correlation values for each of the first N data bursts. For the next M data bursts the receiver estimates the timing location of each data burst based on the average timing location for the first N data bursts.

Fig.5.



EP 0 996 237 A1

Description

Field Of The Invention

[0001] The present invention relates to the tracking of a training sequence in a transmitted radio signal, and particularly but not exclusively to the tracking of training sequences in data bursts in GSM systems. The invention is particularly advantageous when applied in highly noisy environments in which there is a low signal-to-noise ratio.

Background To The Invention

[0002] In any radio communications system inter-symbol interference (ISI) is caused in the radio path by reflections from objects far away from the receive antenna. The symbols become spread out in time and adjacent symbols interfere with each other. The receiver of the radio communications system must then determine the information that was intended to be sent.

[0003] In a GSM system, data is transmitted in bursts, which are placed within timeslots. A training sequence of a known pattern and with good autocorrelation properties is placed in the middle of the data burst. The training sequence is placed in the middle of the burst in order to provide correct channel estimation for the first and the second half of the burst. The position of the received burst in time varies from burst to burst, due to changes in the propagation channel and movement of the mobile station.

[0004] In a GSM system a channel equaliser is provided in the receiver. The purpose of the equaliser, placed in the path of the received signal, is to reduce the ISI and multi-path effects as much as possible to maximise the probability of correct decisions. The channel equaliser uses the training sequence in the burst to equalise the multi-path effects. In order to perform the equalisation effectively, the receiver must first identify the exact position of the training sequence.

[0005] The training sequence is used by the equaliser to create a channel model, which changes all the time but which during one burst can be regarded as constant for a slowly varying channel in time. If two similar interfering signals arrive at the receiver at almost the same time, and if their training sequences are the same, there is no way to distinguish the contribution of each to the received signal. For this reason, different training sequences are allocated to channels using the same frequencies in cells that are close enough so that they do not interfere. When two training sequences differ, and are as little correlated as possible, the receiver can much more readily determine the contribution of each to the received signal.

[0006] The receiver knows the training sequence which the transmitter of the radio communications system transmits, and stores such training sequence. By correlating the stored training sequence with the training sequence received from the transmitter, the channel impulse response of can be measured. The equaliser creates a model of the transmission channel and calculates the most probable receiver sequence.

[0007] Conceptually, the equaliser takes the different time-dispersed components, weighs them according to the channel characteristics, and sums them after inserting the appropriate delay between components, so that a replica of the transmitted signal is restored.

[0008] The problem in cellular radio becomes more complex due to the dynamic nature of the channel. As the mobile moves through multipath surroundings, the equaliser must continually adapt to the changed channel characteristics. The equaliser knows the transmitted training sequence, and also knows what it has actually received. Thus, the equaliser can make an estimate of the channel transfer function. Thus an adaptive equaliser continuously updates the transfer function estimate, making sure that the decision error does not increase too much during the channel transmission.

[0009] In conventional systems, timing estimation is obtained by correlating a data burst with a training sequence stored in the base station. The base station knows the training sequence used by the mobile station. Correlations are performed at various bit positions of the received signal. The bit position that provides the highest correlation value is determined to be the first bit of the training sequence. The received data burst can then be effectively equalised to compensate for the channel.

[0010] However, this known technique suffers significantly from the effects of multipath delays in very noisy environments in which there is a low signal-to-noise ratio. Performing the correlation before the equalisation leads to errors in timing estimation, and hence bit errors at the output of the equaliser.

[0011] It is therefore an object of the present invention to provide an improved technique for estimating the timing position of received data bursts, which operates reliably even in noisy environments.

Summary of The Invention

[0012] According to the present invention, in one aspect there is provided a method of estimating the timing position of data bursts received in a data stream, each data burst including a number of bits comprising a training sequence in a fixed location, the method comprising the steps of: for each of the first N received data bursts: determining a plurality of estimated timing locations of the training sequence; correlating the training sequence for each estimated timing location; determining the timing location associated with the highest correlation value; determining the average timing location of the highest correlation values for each of the first N data bursts; and for the next M data bursts: estimating the timing location of each data burst based on the average timing location for the first N data bursts.

[0013] There is thus provided a technique for estimating the timing position of data bursts which offers significant performance improvements in noisy environments.

[0014] Preferably the method further comprises the steps of: for each of the first N data bursts, equalising the data burst based on the timing location associated with the highest correlation value; and for the next M bursts, equalising each data burst based on the average timing location determined for the first N data bursts.

[0015] Preferably the method further comprises the step of determining the average timing location includes allocating a weighting to each timing location associated with the highest correlation values.

[0016] The weighting is preferably allocated to each timing location in dependence on the level of the associated correlation value.

[0017] In a further aspect the invention provides a receiver for synchronising data bursts received in a data stream, each data burst including a number of bits comprising a training sequence in a fixed location, the receiver including circuitry for estimating the timing position of the data bursts received in the data stream, wherein for each of the first N received data bursts, the receiver estimates a plurality of timing locations of the training sequence, correlates the training sequence for each estimated timing location, determines the timing location associated with the highest correlation value, and determines the average timing location of the highest correlation values for each of the first N data bursts; and for the next M data bursts the receiver estimates the timing location of each data burst based on the average timing location for the first N data bursts.

Brief Description Of The Drawings

[0018]

Figure 1(a) shows the structure of a data stream of a GSM system comprising a number of data bursts;
Figure 1(b) shows the structure of a GSM normal data burst;
Figure 2 is a block diagram illustrating the main components of a conventional circuit for performing equalisation of a GSM data burst;
Figure 3 is flow diagram illustrating the operation of the circuit of Figure 2;
Figure 4 is a block diagram illustrating the main components of a circuit for performing the equalisation of a GSM data burst according to the present invention; and
Figure 5 is a flow diagram illustrating the operation of the circuit of Figure 4.

Description of Preferred Embodiment

[0019] Referring to Figure 1(a) there is shown an overview of the basic structure of a typical GSM transmitted signal. As can be seen, the transmitted signal comprises a plurality of data bursts 2a to 2n. There are five different kinds of bursts in a GSM system: normal burst, synchronisation burst, frequency correction burst, access burst, and dummy burst. Each burst is 156.25 bits long. The present invention applies to any burst containing a training sequence for equalising the burst. The length of the training sequence varies according to the type of data burst. In a normal data burst the training sequence is 26 bits long.

[0020] In practice, transmitted messages are preceded by access bursts during the set-up phase of a transmission. The receiving station therefore initially seeks a training sequence of an access burst. Thereafter, the message includes a plurality of normal data bursts, and the receiving station seeks a training sequence of a normal data burst. The extraction of bursts from a transmitted message will be well understood by one skilled in the art and is outside the scope of the present invention.

[0021] Referring to Figure 2(b), it can be seen that each normal data burst comprises a header portion 4, a first data portion 6a, a training sequence 8, a second data portion 6b, and a tail portion 10. The format and generation of each portion of the data burst of Figure 1(a) will be well known to those skilled in the art.

[0022] Referring to Figure 2, there is shown a block schematic of equalisation circuitry for performing the conventional equalisation process in the receiver of a GSM mobile and GSM Base Station.

[0023] The equalisation circuitry receives a data stream including data bursts as illustrated in Figure 1 on a signal line 46 from the receive antenna. The equalisation circuitry outputs the equalised data stream to be further processed in the receiver on a signal line 48.

[0024] The receive antenna, and the pre-processing circuitry (such as down-converter) which the received signal must go through prior to equalisation is not shown in Figure 2. Such circuitry is beyond the scope of the present invention and the implementation thereof will be within the capabilities of one skilled in the art.

[0025] The equalisation circuitry includes a control circuit 32, a training sequence storage circuit 30, a correlator 40, a set of registers 42, an equaliser 44, a storage circuit 36, a comparator circuit 38, a counter 34, and a value store 35.

[0026] The operation of the circuitry of Figure 2 will now be described in conjunction with the flow diagram of Figure 3, which illustrates the steps performed in a conventional equalisation process.

[0027] The equalisation circuit receives the stream of data on signal line 46, and the received stream of data is shifted into the set of registers 42 under the control of a signal line 70 from the control circuit 32. The set of registers 42 are capable of storing a number of bits in excess of the number of bits in a data burst.

[0028] When the control circuit 32 has filled the set

of registers 42 with the incoming data stream, in a step 12 of Figure 3 the control circuit sets a signal on line 60 to set a value i in the counter 34. The value i in the counter is the bit position of the data stored in the set of registers 42 which it is estimated by the receiver is the first bit of the training sequence of the first data burst. This estimate of the bit position is predetermined.

[0029] In a next step 14, the receiver transfers the contents of the bit location i, and the next successive 25 bit locations of the received data stream (which comprise the 26 bits of the estimated training sequence in a GSM normal data burst), into the correlator 90 from the set of registers 42 via 26 bit parallel signal lines 54 under the control of the signals 70. The correlator also receives, on 26 bit parallel signal lines 52 the training sequence stored in the receiver in the training sequence storage circuit 30, which is the training sequence which the receiver expects to receive.

[0030] The correlator 40 then correlates, in a step 16, the estimated training sequence on parallel lines 54 with the stored training sequence on parallel lines 50. The receiver will therefore correlate the bit i and the next successive 25 bits of the received signal with the 26 bits of the training sequence storage circuit 30.

[0031] The result of this correlation is output on line 64, and in a step 18 the result is stored in the storage circuit 36 under the control of the signal 72 from the control circuit.

[0032] The control circuit 32 of the receiver then determines, in a step 20, whether the value i in the counter 34 is equal to a value n stored in the value store 35 and read on line 63. The value n is the maximum value of i for which the correlation is to be performed. The control circuit 32 reads the contents of the counter 34 on line 62 and compares it to the stored value n on line 63.

[0033] If the control circuit 32 determines that the value i has not yet reached the value n, then the receiver moves onto step 22 and increases the value i in the counter 32 by setting the signal on line 60 as illustrated by step 22 in Figure 3. The amount by which the value i is incremented will be predetermined.

[0034] The steps 14 to 20 of Figure 3 hereinbefore described are then repeated, but with a different value of i such that a different estimate of the training sequence is output on line 54 and correlated with the contents of the training sequence storage circuit.

[0035] When the value i equals the value n in step 20 of Figure 3, the control circuit 32 of the receiver controls the comparator circuit 38 via line 74 to compare the stored correlation values in the storage circuit 36. The stored correlation values are presented to the comparator circuit 38 on lines 66 under the control of control circuit 32 via line 72. This is illustrated by step 24 in Figure 3. The comparator circuit compares the stored correlation results and determines the highest value.

[0036] The storage circuit 36 stores the correlation results together with the value i for which the correlation was performed. The comparator outputs the value i of the highest correlation result to the control circuit 32 on line 76. The correlation result that returns the highest value is estimated to be the value of i that is the first bit of the training sequence of the first data burst.

[0037] In a step 26 the control circuit 32 outputs the set of bits forming the first data burst from the set of registers associated with a training sequence having a first bit in the bit position i. This data burst is output on the lines 56 to the equaliser 44.

[0038] For instance, in the example described of a GSM normal data burst, the data burst is 156.25 bits long, and the first bit of the training sequence is the 62nd bit of the normal data burst. The control circuit therefore can determine the first bit of the data burst once it knows the location of the first bit of the training sequence, and can select all the bits of the data burst. If, say, 200 bits have been stored in the set of registers 42, the control circuit selects the 156.25 bits of the normal data burst.

[0039] Responsive to a control signal on line 73 from the control circuit 32, the equaliser 44 then equalises the received data burst. The data burst is equalised by the equaliser in a known manner in accordance with standard techniques to compensate for the propagation path of the channel. The equalised received data burst is then output on line 48 from the equaliser 44.

[0040] The equalisation process removes the multipath effects from the received signal. That is, the equalisation process eliminates noise from the received signal and produces a clean version of it. The equaliser 44 is a matched filter.

[0041] The control circuit then shifts the first bit received in the set of registers 42 after the last bit of the first normal data burst to the most significant bit position of the set of registers, and then shifts in a further set of received bits into the set of registers until they are full. The above-described steps are then repeated to identify the training sequence of the second and further data bursts.

[0042] In the foregoing description the correlaton was described as performed on 26 bits selected from the received data on the basis that the example described was a normal data burst having a 26 bit raining sequence. It will be appreciated that the control circuit 32 will be controlled by a processor in the receiver such that if the incoming data burst is identified as a different type of burst having a different number of bits in the training sequence, the number of bits correlated will be altered and the training sequence stored in the training sequence storage circuit adjusted.

[0043] The conventional correlation and equalisation technique described hereinabove with reference to Figures 2 and 3 may be applied in any receiver, whether the receiver is in a mobile station or a base station.

[0044] The operation of the improved equalisation technique according to the present invention will now be described with reference to Figures 4 and 5.

[0045] Referring to Figure 4, there is shown a block schematic of circuitry for performing the equalisation process in the receiver of a GSM mobile or a GSM Base Station according to the present invention. Like reference numerals are used in Figure 4 to illustrate elements which correspond to elements shown in Figure 2. The equalisation circuit of Figure 4 additionally includes counters 80 and 86, and value stores 81 and 85.

[0046] The receiver receives the data stream including data bursts as before on line 46, and outputs the equalised data bursts as before on line 48.

[0047] In an initial step 100, the control circuit sets the contents j of the counter 80 to 1 via line 82 on receipt of the first normal data burst. The counter 80 counts the number of data bursts received by the equalisation circuitry.

[0048] The equalisation circuit receives the stream of data on signal line 46, and the received stream of data is shifted into the set of registers 42 under the control of a signal line 70 from the control circuit 32. The set of registers 42, as before, are capable of storing a number of bits in excess of the number of bits in a data burst.

[0049] When the control circuit 32 has filled the set of registers 42 with the incoming data stream, in a step 102 of Figure 5 the control circuit sets a signal on line 60 to set a value i in the counter 34. The value i in the counter is the bit position of the data stored in the set of registers 42 which it is estimated by the receiver is the first bit of the training sequence of the first data burst. This estimate of the bit position is predetermined.

[0050] In a next step 104, the receiver transfers the contents of the bit location i, and the next successive 25 bit locations of the received data stream (which comprise the 26 bits of the estimated training sequence in a GSM normal data burst), into the correlator 90 from the set of registers 42 via 26 bit parallel signal lines 54 under the control of the signals 70. The correlator also receives, on 26 bit parallel signal lines 52 the training sequence stored in the receiver in the training sequence storage circuit 30, which is the training sequence which the receiver expects to receive.

[0051] The correlator 40 then correlates, in a step 106, the estimated training sequence on parallel lines 54 with the stored training sequence on parallel lines 50. The receiver will therefore correlate the bit i and the next successive 25 bits of the received signal with the 26 bits of the training sequence storage circuit 30.

[0052] The result of this correlation is output on line 64, and in a step 108 the result is stored in the storage circuit 36 under the control of the signal 72 from the control circuit.

[0053] The control circuit 32 of the receiver then determines, in a step 110, whether the value i in the counter 34 is equal to a value n stored in the value store 35 and read on line 63. The value n is the maximum value of i for which the correlation is to be performed. The control circuit 32 reads the contents of the counter 34 on line 62 and compares it to the stored value n on line 63.

[0054] If the control circuit 32 determines that the value i has not yet reached the value n, then the receiver moves onto step 112 and increases the value i in the counter 32 by setting the signal on line 60. The amount by which the value i is incremented will be predetermined.

[0055] The steps 104 to 108 of Figure 5 hereinbefore described are then repeated, but with a different predetermined value of i such that a different estimate of the training sequence is output on line 54 and correlated with the contents of the training sequence storage circuit.

[0056] When the value i equals the value n in step 110 of Figure 5, the control circuit 32 of the receiver controls the comparator circuit 38 via line 74 to compare the stored correlation values in the storage circuit 36. The stored correlation values are presented to the comparator circuit 38 on lines 66 under the control of control circuit 32 via line 72. This is illustrated by step 114 in Figure 5. The comparator circuit compares the stored correlation results and determines the highest value.

[0057] The storage circuit 36 stores the correlation results together with the value i for which the correlation was performed. The comparator outputs the value i of the highest correlation result to the control circuit 32 on line 76. The correlation result that returns the highest value is estimated to be the value of i that is the first bit of the training sequence of the first data burst. In a step 116 the control circuit 32 outputs the set of bits forming the first data burst from the set of registers 42 associated with a training sequence having a first bit in the bit position i. This data burst is output on the lines 56 to the equaliser 44.

[0058] Responsive to a control signal on line 73 from the control circuit 32, the equaliser 44 then equalises the received data burst. The data burst is equalised by the equaliser in a known manner in accordance with standard techniques to compensate for the propagation path of the channel. The equalised received data burst is then output on line 48 from the equaliser 44.

[0059] After the equalisation step 116, in a step 118 the control circuit stores the correlation value of the equalised, output data burst in the storage circuit 36, together with the value i for which the data burst was equalised.

[0060] Then, in a step 120, the control circuit 32 checks the contents of the counter 80. In the step 120 the control circuit 34 reads the contents of the counter 80 on line 84 and compares it to a value N in value store 81. If the value j of the counter 80 does not equal the value N of the value store 81 then the control circuit proceeds to step 122.

[0061] In step 122 the control circuit increments the value j of the counter 80 by one by setting line 82. The control circuit 32 then, in step 104, inputs the next set of bits into the set of registers 42 that will form the second

(j=2) data burst.

[0062] Again, the receiver selects a bit of the data stream as being a first possible candidate for the first bit of the training sequence of the second data burst based on the current value i in the counter 34. The bit location i is reset to the first predetermined value in step 122.

[0063] The steps 104 to 108 are then repeated, as before, until the value of i reaches n. Thus the second and successive data bursts are correlated for the same series of values of i.

[0064] As before, the receiver synchronises the data stream based on the correlation value determined in step 114 to be the highest, and equalises the thus synchronised data burst in the step 116. The correlation value and value of bit i for the equalised data burst are again stored in the storage circuit 36 for the output equalised data burst.

[0065] The steps described above are repeated for successive data bursts until the value j equals the value N in step 120. The receiver thus repeats the steps on the first N data bursts received.

[0066] When, in step 120, the value j stored in the counter 80 reaches the value N, the control circuit moves onto a step 122, in which the correlation value of all j data bursts that have been equalised are evaluated. The bit positions i associated with each of the j equalised data bursts, stored in steps 118, are averaged to determine the position, on average, of the first bit of the training sequence for the first j data bursts equalised. The average value of i is then stored in storage circuit 36.

[0067] The control circuit then uses the average value of i for the first j data bursts as giving the best estimate as to the correct location of the first bit of the training sequence for the next M data bursts.

[0068] The step 122 may also include a weighting function in determining the average value of i. That is, the values of i may be weighted in accordance with the strength, or energy, of the correlation result with which they are associated.

[0069] In a next step 124, the control circuit sets a value k in value store 86 to (N+1) by setting line 83. In a step 146 the control circuit 32 then inputs into the set of registers 42 the kth, ie the (N+1)th, data burst.

[0070] The kth data burst is synchronised in a step 128 according to the estimation for the location of the first bit of the training sequence made based on the average calculation made for the first N data bursts.

[0071] In a step 130, the (N+1)th data burst is then equalised and output on line 48. Thus no timing estimation is performed on the (N+1)th data burst.

[0072] In a step 134, after equalisation, the control circuit 34 reads the value k of the counter 86 on line 88 and determines whether the value k matches a stored value M in value store 85 on line 87. If k does not equal M, then the value (N+1) of k in the counter 86 is incremented, in step 115, by one by setting line 88 and the next data burst, ie the (N+2)th, is input into the set of registers 42.

[0073] The steps 126 to 134 are then repeated for the next M data bursts. That is for the next M data bursts the timing estimation based on the first N data bursts is used, no correlation being performed on these data bursts, only equalisation.

[0074] When the (N+1+M)th data burst is received, k=M in step 118 and the receiver reverts back to step 100 and the same estimation technique performed on the first N data bursts, and so the procedure is cyclical.

[0075] Thus, once the initial N bursts have been used to determine the timing of the received signal, only equalisation is performed on the following M data bursts.

[0076] The value of M depends upon both the speed of the mobile station concerned and the rate of change in the propagation channel. Normally the effects of the former far outweigh the latter. A value of M= 100 may be typically chosen, against a typical value of N=8.

[0077] During the first N data bursts bit errors may occur. This can be alleviated by reducing N after some initial equalisations if the propagation channel does not change significantly. In reality, 8 data bursts (N=8) lasts about 5ms, and it is hardly noticeable even if all 8 data bursts are erased from any speech.

[0078] Because of constraints on processing and power resources, it is likely that the technique of the present invention will currently be applied only in communication system base stations. Employing the invention in current mobile stations would require additional processing capabilities, which are not currently available. However it is envisaged that future mobile stations will be able to support the present invention when the required processing and power capabilities are incorporated in mobile stations.

Claims

1. A method of estimating the timing position of data bursts received in a data stream, each data burst including a number of bits comprising a training sequence in a fixed location, the method comprising the steps of:

    for each of the first N received data bursts:

        determining a plurality of estimated timing locations of the training sequence;
        correlating the training sequence for each estimated timing location;
        determining the timing location associated with the highest correlation value;

    determining the average timing location of the highest correlation values for each of the first N data bursts; and
    for the next M data bursts:

estimating the timing location of each data burst based on the average timing location for the first N data bursts.

2. The method of claim 1 further comprising the steps of:

   for each of the first N data bursts, equalising the data burst based on the timing location associated with the highest correlation value; and

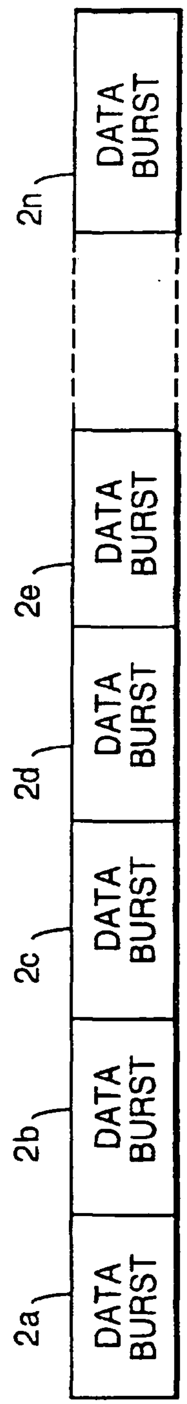
   for the next M bursts, equalising each data burst based on the average timing location determined for the first N data bursts.

3. The method of claim 1 or claim 2 wherein the step of determining the average timing location includes allocating a weighting to each timing location associated with the highest correlation values.

4. The method of claim 3 wherein the weighting is allocated to each timing location in dependence on the level of the associated energy level.

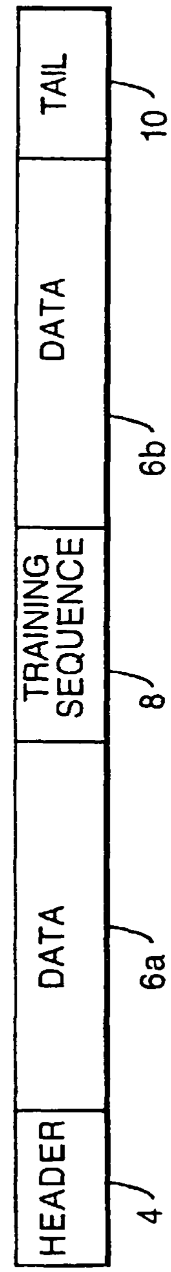
5. A receiver for synchronising data bursts received in a data stream, each data burst including a number of bits comprising a training sequence in a fixed location, the receiver including circuitry for estimating the timing position of the data bursts received in the data stream, wherein for each of the first N received data bursts, the receiver estimates a plurality of timing locations of the training sequence, correlates the training sequence for each estimated timing location, determines the timing location associated with the highest correlation value, and determines the average timing location of the highest correlation values for each of the first N data bursts; and for the next M data bursts the receiver estimates the timing location of each data burst based on the average timing location for the first N data bursts.

6. A communications system including the receiver of claim 5.



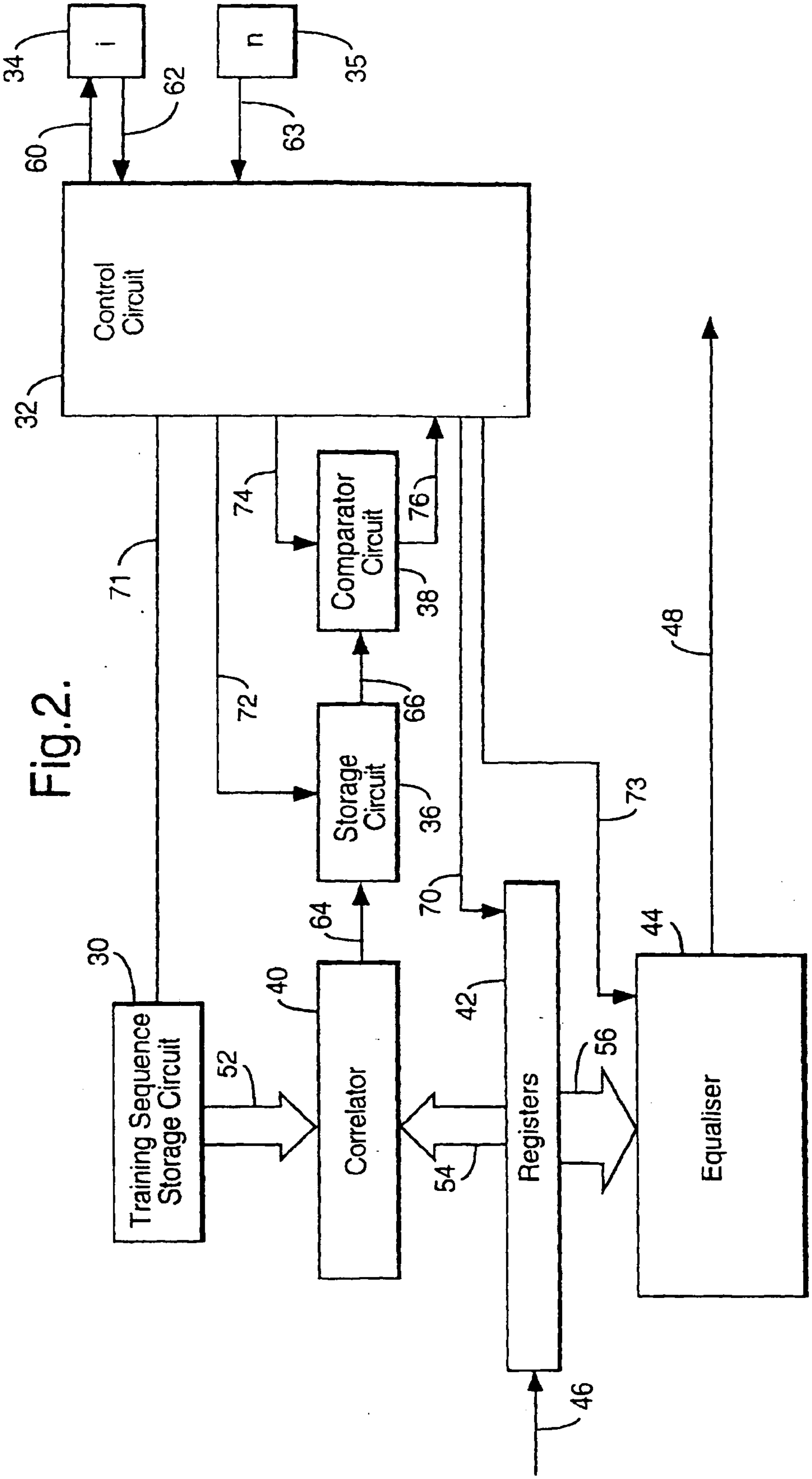
2a
DATA BURST
2b
DATA BURST
2c
DATA BURST
2d
DATA BURST
2e
DATA BURST
2n
DATA BURST

Fig.1(a).



HEADER
4
DATA
6a
TRAINING SEQUENCE
8
DATA
6b
TAIL
10

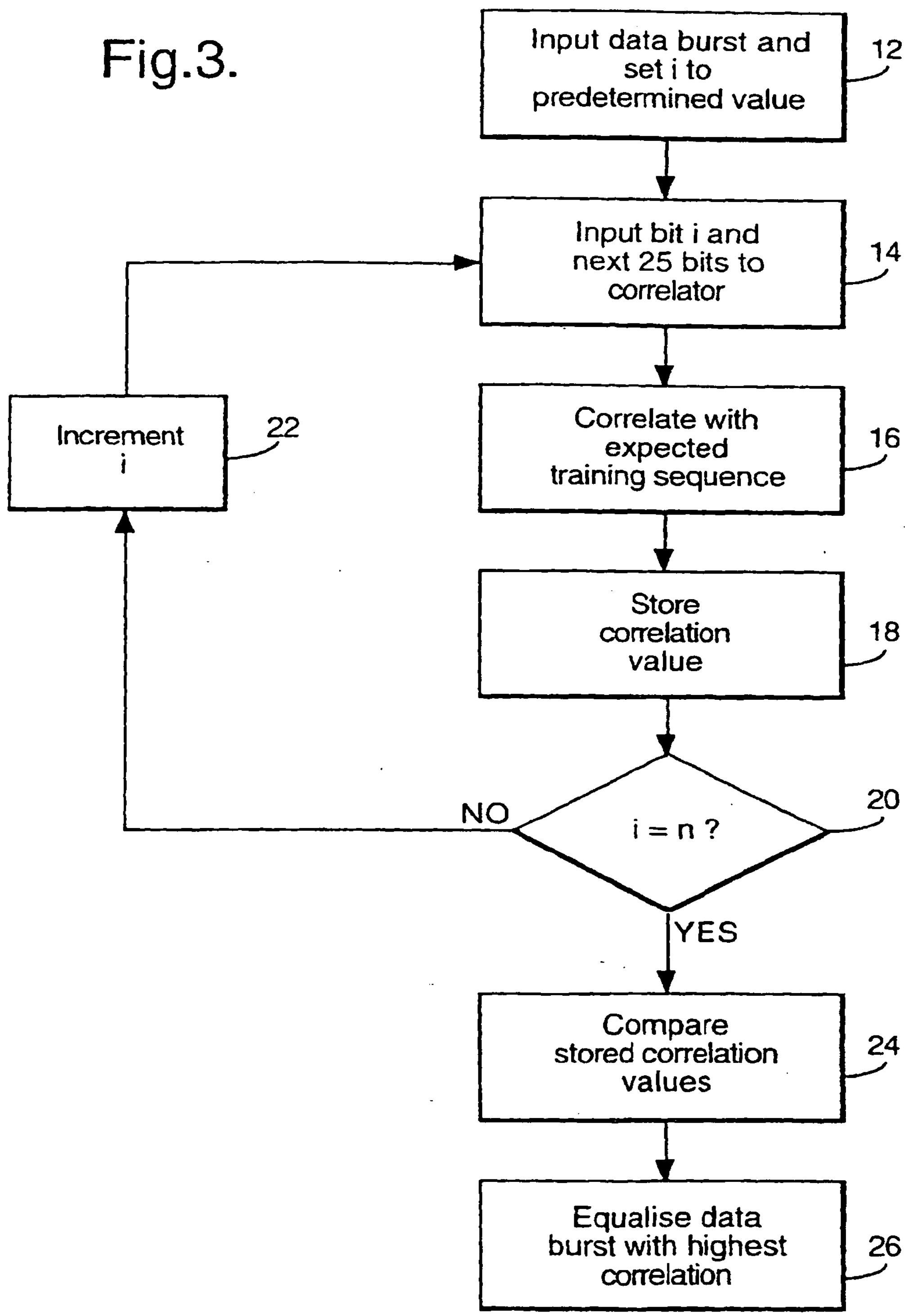
Fig.1(b).



i
n
34
35
60
62
63
Control
Circuit
32
71
72
74
76
Comparator
Circuit
38
66
Storage
Circuit
36
73
48
70
30
Training Sequence
Storage Circuit
40
64
42
44
52
Correlator
54
Registers
56
Equaliser
46

Fig.2.

Fig.3.


Input data burst and set i to predetermined value
12
Input bit i and next 25 bits to correlator
14
Correlate with expected training sequence
16
Store correlation value
18
i = n ?
20
NO
YES
Increment i
22
Compare stored correlation values
24
Equalise data burst with highest correlation
26

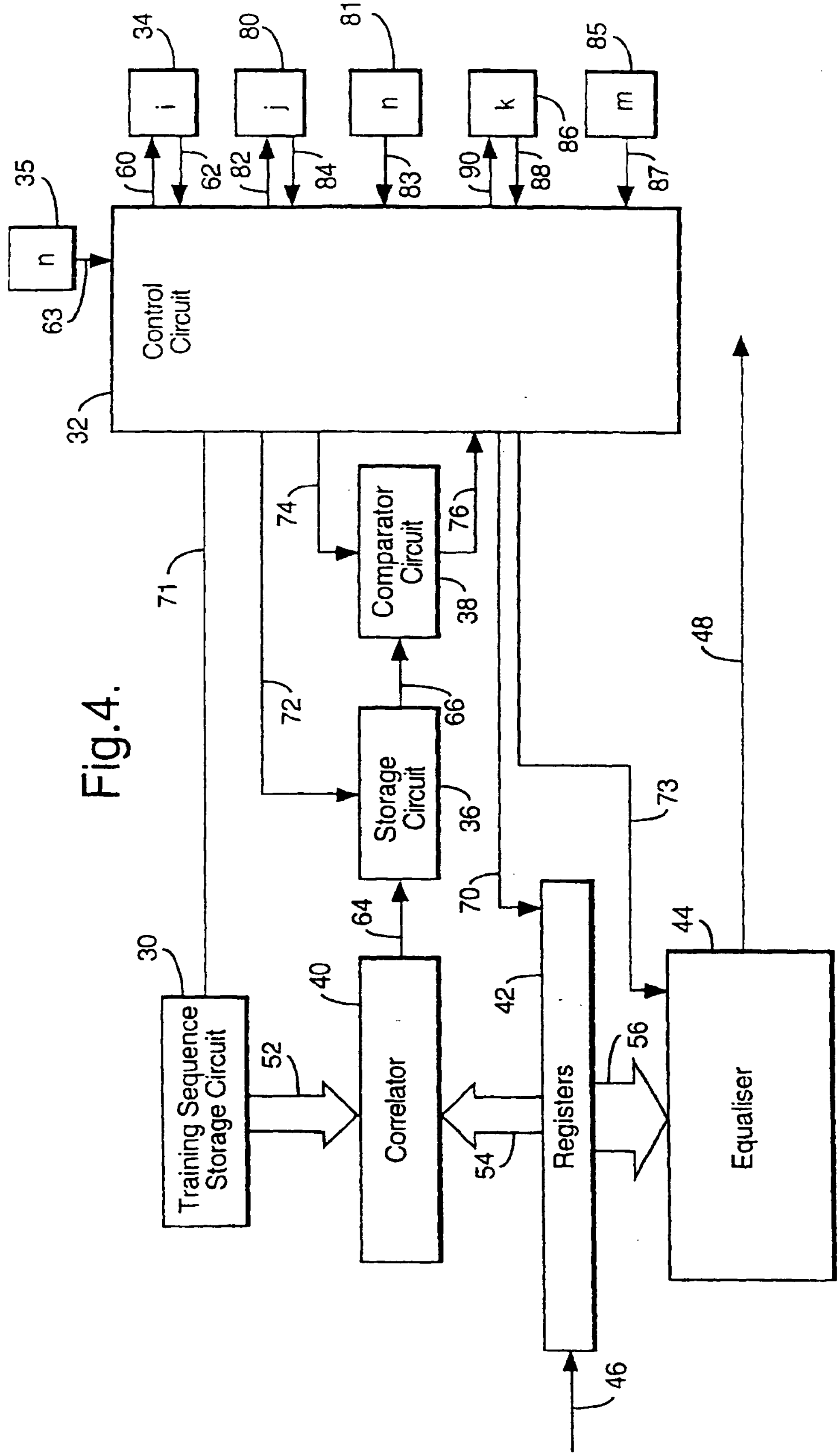

Training Sequence Storage Circuit
Correlator
Registers
Equaliser
Storage Circuit
Comparator Circuit
Control Circuit
i
j
n
k
m
n
30
32
34
35
36
38
40
42
44
46
48
52
54
56
60
62
63
64
66
70
71
72
73
74
76
80
81
82
83
84
85
86
87
88
90

Fig.4.

Fig.5.

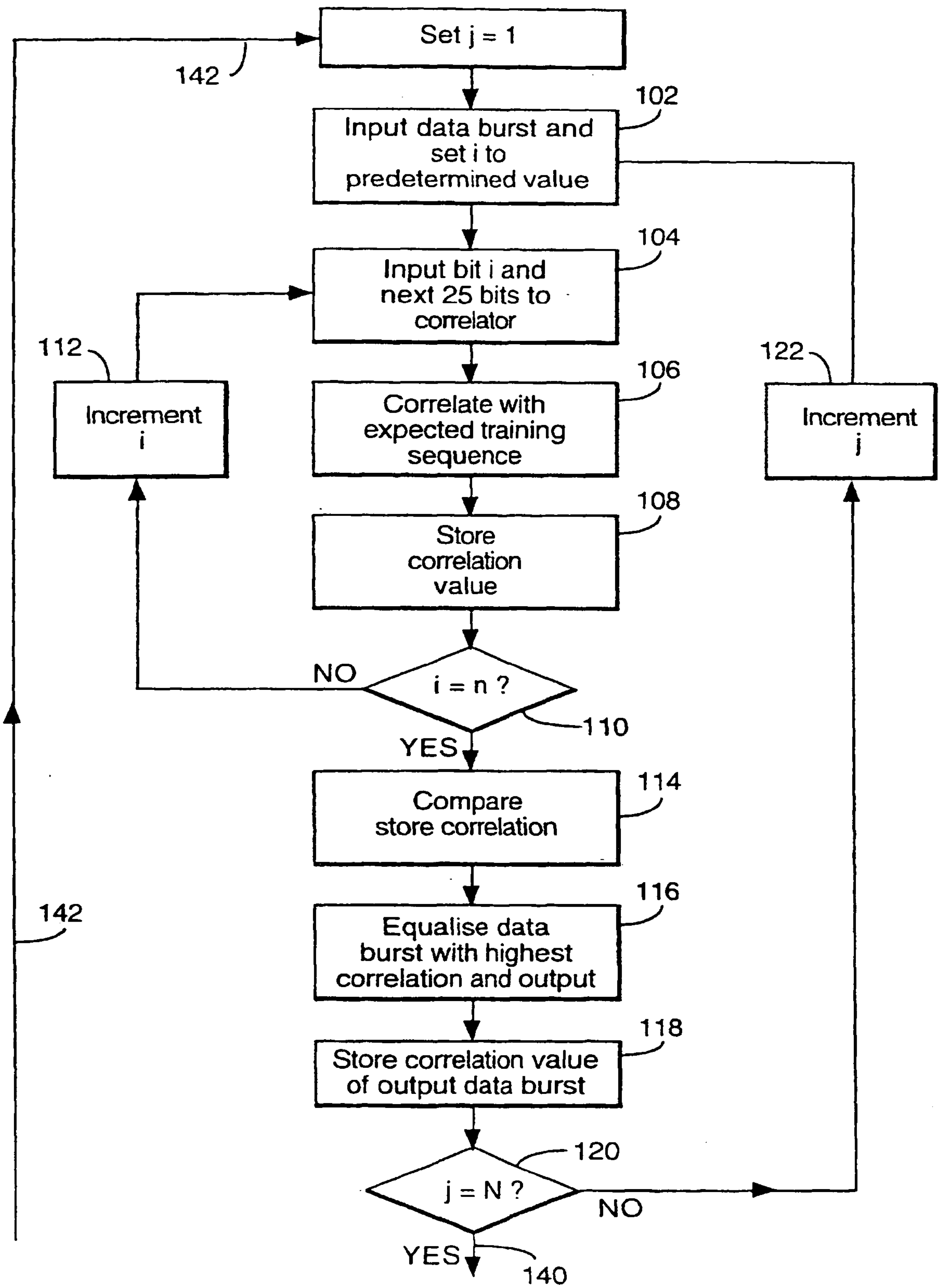
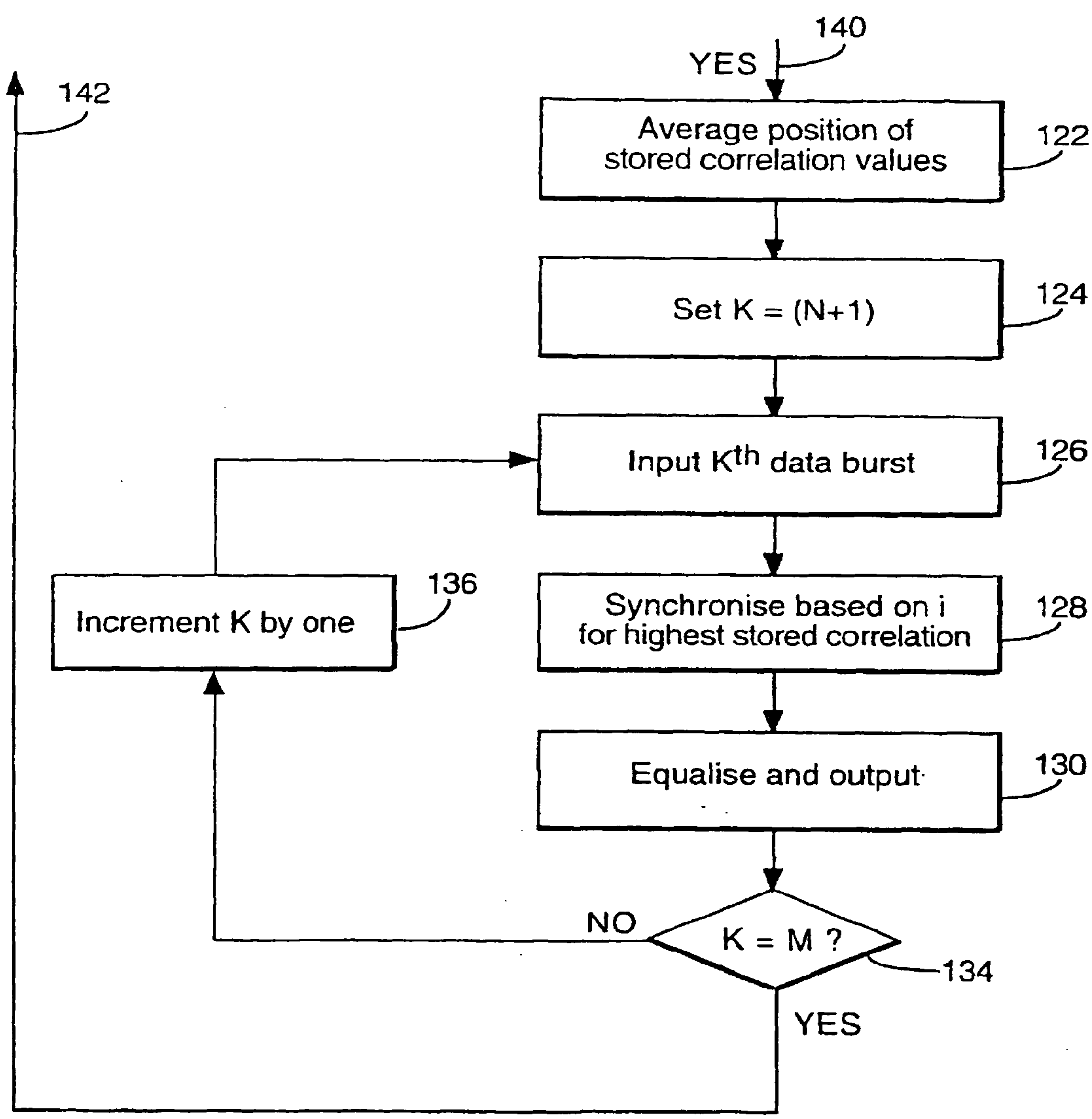

Set j = 1
142
102
Input data burst and set i to predetermined value
104
Input bit i and next 25 bits to correlator
112
Increment i
106
Correlate with expected training sequence
122
Increment j
108
Store correlation value
NO
i = n ?
110
YES
114
Compare store correlation
116
Equalise data burst with highest correlation and output
142
118
Store correlation value of output data burst
120
j = N ?
NO
YES
140

Fig .5 (Cont.)


140
YES
142
Average position of stored correlation values
122
Set K = (N+1)
124
Input Kth data burst
126
Increment K by one
136
Synchronise based on i for highest stored correlation
128
Equalise and output
130
NO
K = M ?
134
YES

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 30 8514

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
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H04B
H04L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	11 March 1999	Burghardt, G

CATEGORY OF CITED DOCUMENTS

X particularly relevant if taken alone
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T theory or principle underlying the invention
E earlier patent document, but published on, or after the filing date
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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 98 30 8514

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11-03-1999

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82